REMARKS

These remarks are in response to the Office Action mailed on October 8, 2003. The Applicants thank the Examiner for indicating the allowability of claims 14-32 and 45-58. The Office Action rejected claims 1, 3, 4, and 33, along with their dependent claims under 35 U.S.C. 112, second paragraph, and rejected claims 1 and 2 under 35 U.S.C. 102(b) as anticipated by Lee (U.S. patent number 6,480,419). As noted below, although it is respectfully submitted that the rejections under U.S.C. 112, second paragraph, are not well founded, claims 1, 3, 4, and 33 have been amended to facilitate the application process. As is also discussed below, it is believed that the rejection of claims 1 and 2 under 35 U.S.C. 102(b) is also not well founded.

Rejections under U.S.C. 112, second paragraph

The Office Action rejected claims 1, 3, 4, and 33, along with their dependent claims under 35 U.S.C. 112, second paragraph, due to the use of "can be" as not providing a positive limitation. Although it is believed that, as used in this claims, "can be" is not a conditional but rather a positive usage, claims 1, 3, 4, and 33 have been reworded to overcome these rejections.

Rejections under U.S.C. 102(b)

The Office Action rejected claims 1 and 2 under 35 U.S.C. 102(b) as anticipated by Lee (U.S. patent number 6,480,419). The relevant parts of claim 1 (where the emphasis is added) reads:

> ... a plurality of storage units formed upon a substrate and arranged into a plurality of columns connected along respective bit lines each comprising a number of said a number of said *storage units connected in series between a first select transistor and a second select transistor*;
>
> ...and
>
> biasing circuitry connected to the select transistors, whereby *the voltage level on the gates of the first select transistors in one subset is settable independently of the voltage level on the gates of the first select transistors in the other subsets and the voltage level on the gates of the second select transistors in one subset is settable independently of the voltage level on the gates of the second select transistors in the other subsets.*

An exemplary embodiment of this structure is shown in Figure 2b of the present application, showing "a number of ... storages units [such as the string floating gate transistors connected to wordlines WL0-WL15, taken individually or collectively] connected in series between a

first select transistor and a second select transistor [the transistors on either end of the string connected to SGD and SGS]". The voltage level on the two select transistors in one set (such as the left set with signals SGDL and SGSL) can be set independently of the select transistors in the other set (such as the right set with signals SGDR and SGSR).

Referring to Figure 2 of Lee, the Office Action identifies the "select transistors" of the claim with transistors 102e and 122e for one set and with transistors 102o and 122o for the other set. The Office Action is correct in that the voltage levels on these two sets of transistors can be set independently; however, these transistors do not meet the requirements of the "select transistors" as specified in the claim. The first element of the claim states the "*storage units* [are] *connected in series between a first select transistor and a second select transistor*", where the emphasis is again added. The Office Action identifies the storage units as the NAND strings 112e and 112o; however, these storage units are ***not*** connected in parallel between 102e and 122e (for 112e) and 102o and 122o (for 112o). As can be seen in Figure 2 of Lee, it is only the node at the top of these storage units that is connected between what the Office Action identifies as the select transistors, the storage units themselves are not "connected in series between a first select transistor and a second select transistor".

(If instead, the storage units are identified as M0-MM, either individually or collectively, then they are connected in series between ST (or 102) and GT; but all of the GT transistors in both the even and odd groups have their gates connected together and receive the same signal GSL. The voltage level on the odd GT transistors is not settable independently of the voltage on the even GT transistors.)

With respect to claim 2, this states that "each of said subsets of columns are formed upon a distinct contiguous region of the substrate." This is not the case for the sort of embodiment shown Figure 2 of Lee, where the odd and even subsets are interleaved. Claim 2 is instead drawn to an embodiment such as in Figure 2b of the present application, where there are distinct, but contiguous, left and right regions.

For any of these reasons, it is respectfully submitted that the Office Action's rejection claims 1 and 2 under 35 U.S.C. 102(b) as anticipated by Lee is not well founded and that these claims, along with their dependent claims, are allowable over the prior art.

Conclusion

For these reasons, claims 1-13 and 33-44 are believed allowable. Reconsideration of claims 11-13 and 33-44 is respectfully requested and an early indication of their allowability is earnestly solicited. The Applicants would also like to draw the Examiner's attention to an Information Disclosure Statement previously filed on August 15, 2003, of which there is no indication of its having been considered, and to a Supplemental Information Disclosure Statement being filed concurrently with the present Amendment.

Respectfully submitted,

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